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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,021	07/09/2003	Jri Lee	G&C 30448.116-US-U1	1118

22462 7590 07/27/2006

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EXAMINER	
WONG, LINDA	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 07/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,021	LEE ET AL.	
	Examiner	Art Unit	
	Linda Wong	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. The affidavit filed on 4/25/2006 under 37 CFR 1.131 is sufficient to overcome the Song et al (Publication: "4-G/bs Clock and Data Recovery Using Four-Phase 1/8-Rate Clock") reference.

Response to Arguments

2. Applicant's arguments, see Applicant's Remarks, filed 4/25/2006, with respect to the rejection(s) of claim(s) 1-20 under Song et al have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Wurzer et al (Publication: "A 40-Gb/s Integrated Clock and Data Recovery Circuit in a 50-GHz f_T Silcon Bipolar Technology") in view of Shimoda (US Patent No.: 5373257).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1-2,4-6,11-12,14-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wurzer et al (Publication: "A 40-Gb/s Integrated Clock and Data

Recovery Circuit in a 50-GHz f_T Silcon Bipolar Technology") in view of Shimoda (US Patent No.: 5373257).

a. **Claims 1 and 11**, Wurzer et al discloses a multi-phase voltage controlled oscillator (VCO) (Fig. 2a, labels vco,clk,90 degree,C3 and C2) for receiving a control signal (Fig. 2a, output from label lpf and page 1321, left col., lines 1-4) changing the phase, which due to the relationship between phase and frequency, inherently changes the frequency of a clock signal output (Fig. 2a, label vco,clk,90 degree, c3 and c2),

- a phase detector (Fig. 2a, labels dff1,dff2,dff3, xor) for sampling the input data signal (Fig. 2a, labels din,d1,d2,d3) using the clock signal received from the VCO (Fig. 2a, labels c3 and c2) and generating a plurality of output data signals (Fig. 2a, labels D1,D2,D3), wherein the input data signal would inherently have a frequency different from the frequency of the clock signal since the purpose of clock and data recovery circuit is to detect the differences between the two inputs and make corrections (page 1321, left Col., lines 5-17) and the input data signal is retimed and demultiplexed (Fig. 2, labels D1, D2,D3 and demux) into the output data signals (Fig. 2a, labels D1,D2,D3) by the phase detector (Fig. 2a, label IC) using the plurality of phases of the clock signal (Fig. 2a, labels vco,90 degree,C2,C3) such that each of the output data signals detect an edge or transition of the input data signal and determine whether the edge or transition is early or late (page 1320, left col., section III, page 1321 and page

1321, right col. and Fig. 2b) corresponding the multiple phase clock signals (Fig. 2a, labels C2,C3) and

- a loop filter (Fig. 2a, label lpf and page 1321, left col., lines 1-4) for outputting a control signal to the VCO (Fig. 2a, label output to vco).
- Although Wurzer et al fails to disclose a voltage to current converter and a loop filter receiving the voltage to current converter, Shimoda discloses a loop filter comprising a voltage to current converter for receiving a signal from the phase comparator (Fig. 2, labels 12, 13) and outputting a control signal to the VCO (Fig. 2, labels 13 and 11). It would be obvious to one skilled in the art to incorporate the loop filter as shown in Fig. 2 of Shimoda's invention into Wurzer et al's invention to change the control voltage to the VCO so to adjust the frequency of the output signal of the VCO. (Col. 3, lines 1-10, 32-40, Col. 2, lines 5-24 and lines 59-68)

b. **Claims 2 and 12**, Wurzer et al discloses receiving a single input data signal (Fig. 2a, label Din) and retiming and demultiplexing the input data signal to a plurality of output data signals (Fig. 2a, labels D1,D2,D3).

c. **Claims 4 and 14**, Wurzer et al discloses a phase detector (Fig. 2a, label IC) comprises a plurality of flip-flops (Fig. 2a, labels dff1,dff2,dff3) to strobe the input signal (Fig. 2a, label Din) at intervals based on the plurality of phases of the clock signal (Fig. 2a, labels clk,c2,c3) received from the VCO (Fig. 2a, label vco).

d. **Claims 5 and 15**, Wurzer et al discloses the phase detector (Fig. 2a, label IC) compares every two adjacent or consecutive samples (Fig. 2a, labels xor and D2,D3) stored by two adjacent or consecutive flip flops (Fig. 2a, labels dff1,dff2,dff3) by means of a XOR gate (Fig. 2a, label xor), which generates a difference or net output current if the two consecutive samples are unequal (Fig. 2a, label XORout) thus indicating the edge or transition has occurred in the data signal. (Fig. 2b)

e. **Claims 6 and 16**, Wurzer et al shows in Fig. 2b the transitions or edges in which are used to sample the input data signal based on the clock signals. (Fig. 2b)

4. **Claims 3-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wurzer et al (Publication: "A 40-Gb/s Integrated Clock and Data Recovery Circuit in a 50-GHz f_T Silcon Bipolar Technology") in view of Shimoda (US Patent No.: 5373257) and further in view of Savoj et al (Publication Title: "A 10Gb/s CMOS Clock and Data Recovery Circuit with Frequency Detection").

a. **Claims 3 and 13**, Although Wurzer et al only outputs two phase-shifted clock signals, Savoj et al discloses a VCO outputting a half-quadrature clock signals (Fig. 5.3.1, VCO and outputs), wherein the clock signasl are inputted into a phase detector (Fig. 5.3.1). It would be obvious to one skilled in the art to expand the VCO disclosed in Wurzer et al's invention with Savoj et al's VCO to

provide a clock and data recovery system with less cost and integration issues for a high range signal. (page 1, left column, lines 5-12)

5. **Claims 7-10 and 17-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wurzer et al (Publication: "A 40-Gb/s Integrated Clock and Data Recovery Circuit in a 50-GHz f_T Silcon Bipolar Technology") in view of Shimoda (US Patent No.: 5373257) and further in view of Henrion (US Patent No.: 6690243).

   a. **Claims 7,17**, Although Shimoda and Wurzer et al discloses a multi-phase VCO within the disclosed PLL (Huang, Col. 1, lines 5-9, Fig. 5, outputs from label 21 and Wurzer et al, Fig. 2, labels 90 degree,C3 and C2), Huang and Wurzer et al fails to disclose the structure of the multi-phase VCO. Henrion discloses providing a 45 degree phase shift signal at the oscillation frequency and a ring oscillation structure (Col. 6, lines 47-50), which inherently comprises a phase separation of 180 degrees at diagonally-opposite nodes. (Fig. 3) It would be obvious to one skilled in the art to use the multi-phase VCO as disclosed by Henrion in Huang and Wurzer et al's invention since Huang and Wurzer et al both disclose a multi-phase VCO (Huang, Col. 1, lines 5-9, Fig. 5, outputs from label 21 and Wurzer et al, Fig. 2, labels 90 degree,C3 and C2) to provide an easier design and cheaper VCO.

   b. **Claims 8,18,** Henrion discloses a multiphase VCO with a ring oscillation structure, which inherently has a travel time of a wave around a loop. (Fig. 3, and Col. 6, lines 47-50)

c. **Claims 9,19**, Henrion discloses inductor elements (Fig. 7, label L) are grouped in such a way to show a difference in voltage between two nodes or a differential structure (Fig. 7, inductors in between nodes labeled V0,V180,V90 and V270) and -Gm cells are placed in close proximity to the nodes of the VCO (Fig. 7, labels 152a and 152b).

d. **Claims 10,20**, Henrion discloses each differential port of the VCO (Fig. 7, inputs and outputs from labels 152a and b) is buffered inductively loaded differential pair switches (Fig. 7, inductors between nodes labels V0,V180,V90 and V270).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Cheih Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Linda Wong

KEVIN KIM
PATENT EXAMINER